INTEGRATING SIGNAL PROCESSING AND A/D CONVERSION IN ONE FOCAL-PLANE MOUNTED ASIC

Turning photons into bits in the cold

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Abstract: The CRIC (CCD Readout IC) ASIC has been designed to meet the power, space and radiation requirements of the SNAP satellite. It incorporates four channels consisting of a pre-amplifier, double correlated sampler and pipeline A/D converter with integrated voltage reference. The CRIC chip has been specifically designed to operate both at room temperature and at typical focal plane temperatures down to 130K. This minimizes wiring complexity while maintaining signal integrity on complex focal planes. CRIC is half of a two ASIC CCD readout system; the other ASIC in development is a bias and clock voltage generator. Also in development, are 16 and 32 channel versions of CRIC for use with hybrid photodiode and near infrared pixel arrays.

Key words: ASIC; CCD readout; cryogenic; radiation tolerant; low power

1. INTRODUCTION

A four-channel custom chip designed for reading out charge coupled devices (CCD) is presented. This design is part of the research and development program for the SNAP (Super Nova/Acceleration Probe) project. SNAP is an international satellite proposal dedicated to understanding the dark energy responsible for the accelerating expansion of our universe. It has a 2 meter telescope with a large field of view. CCDs and near infrared detectors are located on the focal plane for imaging and spectroscopy. The primary goal of the CRIC circuit is to cover a 16-bit

dynamic range with a readout noise of 7μV rms (2 electrons) referred to the input at 100kpixel/s readout speed.

The circuit described is intended to operate close to the CCDs in order to reduce interconnect heat-load and complexity as well as minimize pick-up noise. This gives additional constraints to the circuit such as low power consumption, operation at 140K and radiation tolerance to a total dose of 10krad. In order to simplify the testing and characterization of the chip full operation at room temperature is desirable. The chip was designed in standard 0.25μm CMOS technology using only 3.3V transistors. This technology was chosen since it is mature, but far from being obsolescent. The choice of 3.3V transistors also increases the design portability to other foundries, further improving manufacturability and longevity of the circuit design.

This chip described here is CRIC II. CRIC I[1] was a proof-of concept chip that implemented the basic analog signal path of the circuit and was used to validate the signal path architecture and to gain insight into low temperature operation.

2. CIRCUIT OVERVIEW

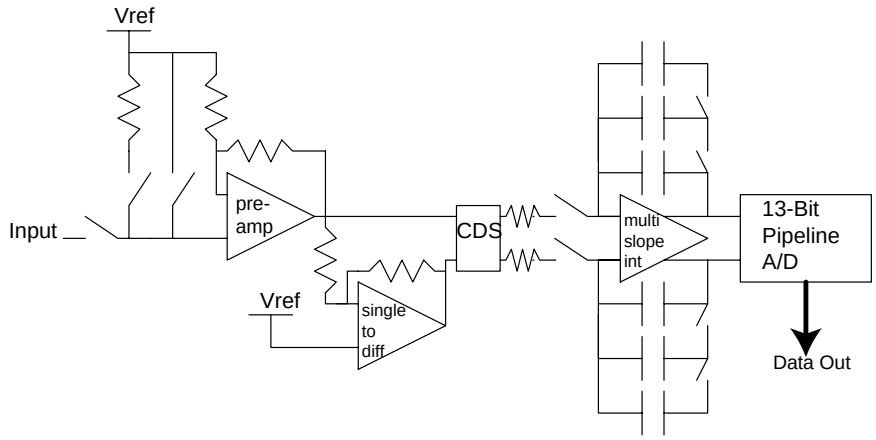

Figure 1. The block diagram of the CRIC II chip.

The circuit consists of four major components, which can be seen in Fig.1:

- The input stage with preamplifier and single-ended to differential conversion.
- The signal processing stage with its Correlated Double Sampler (CDS).
- The Analog to Digital Converter (A/D).
- The band-gap based voltage reference for both the input stage and A/D.

2.1 The input stage

The CCD will be AC coupled to the readout chip with a large external capacitor. This is necessary to eliminate the influence of the parasitic capacitance of the input node due to ESD protection circuitry. To charge this capacitor to its operating voltage upon CCD power-up, the CRIC II has a dedicated input clamp switch that connects its input to the voltage reference with a low resistance. After power-on, the switch is disabled.

During normal operation, two other switches control the input signal. One switch disconnects the input during CCD clocking transitions to prevent amplifier saturation. The last switch is responsible for setting the DC operating point of the input amplifier. During the sampling of the CCD reset level, this switch is closed. It connects the input to the reference voltage through a large (200kΩ) resistor. Together with the input coupling capacitor, this resistance creates a time constant for change of the input voltage that is much longer than a single pixel sampling time. Since the CCD reset level is independent of the CCD signal, averaging over the reset level only creates a consistent DC baseline for the signal processor.

The central part of the input stage consists of an ultra low noise preamplifier with a gain of four. The gain is chosen to minimize the noise contribution of downstream system components, while maintaining a large dynamic range using only 3.3V operating voltage. The opamp input is biased at 200μA to achieve a thermal noise spectral density of about $4nV/Hz^{1/2}$. The output settling time to 16-bit linearity is about 200ns. The input stage is one of the main power consumers of the chip, but lower power can only be achieved at the price of higher noise. The output of the first stage is connected to a unity gain inverter, generating a differential signal of 2V from a 500mV full-scale CCD signal input, effectively doubling the available dynamic range.

2.2 The correlated double sampler

It has been shown[2] that a dual slope integrator is efficient at eliminating reset transistor noise, and also attenuates noise that is significantly higher or lower in frequency than the CCD pixel rate. Such a dual slope integrator

integrates the reset signal level at one polarity and then integrates the image signal level at the opposite polarity, in effect subtracting the reset level from the image level. Since the input stage already generates a differential signal, changing the polarity of the input signal for the integrator merely requires a cross-over switch. Care has to be taken that the resistive miss-match of the switch is much smaller than the integration resistor (see Fig 1.) to obtain the full benefit of the CDS noise rejection.

The gain of the integrator is directly dependant on the value of the integration resistors, while the input stage gain is dependant only on the ratio of feedback resistors. Therefore, the integration resistors require particular attention to reduce the temperature coefficient.

2.3 The multi slope integrator

The dynamic range requirement is 16-bit, derived from 2 electrons CCD readout noise and 130k electrons full well capacity. The requirement for the signal to noise ratio, however, is driven by the Poisson process of the light interacting in the sensor, which has a variance equal to $\sqrt{N}$, where N is the number of incoming photons[3]. The signal can be digitized with an LSB size that depends on the signal amplitude such that the A/D quantization noise is still below the Poisson noise, allowing the implementation of a dynamic range compression without the loss of data. Since the implementation of a radiation tolerant 16-bit A/D converter in the required power budget seemed unrealistic, a means of dynamic range compression had to be adopted. The CRIC chip is intended for use in high precision photometry, so the compression scheme has to allow for simple yet precise calibration.

In the CRIC chip a novel compression was implemented; the integrator has three integration capacitors. Initially only the smallest capacitor is connected. A comparator at the integrator output triggers a flip-flop if the voltage on the integration capacitor rises above a set-point. This switches in an additional, larger capacitor. A third capacitor can be switched in for even larger signals. Fig. 2 shows the signal at the output of the integrator for a signal close to full-scale. On traces two and three the flip-flop outputs that drive the gain selection are shown. These two gain bits are transmitted along with the A/D conversion result for each CCD pixel to allow full reconstruction of the image signal.

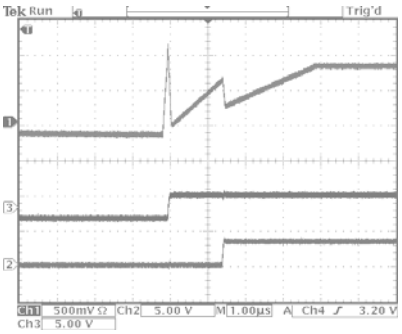

Figure 2. A large signal on the auto-gain integrator.

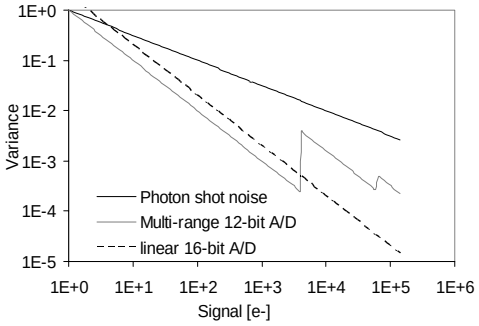

Figure 3. Comparing shot noise and quantization noise.

There are several advantages of a multi-slope integrator over a logarithmic gain amplifier for dynamic range compression. A non-linear preamplifier requires extensive data sets for gain and offset calibration, and radiation induced parameter shifts will likely require on-orbit recalibration. For the multi-slope integrator this is much easier. When the second gain stage is triggered and the additional capacitor is turned on, the charge stored on the integration capacitor is redistributed, but none of it is lost. Additional charge injection from switching is carefully eliminated. This means that in each section the gain is different, yet they all share a common offset. To fully characterize the system one needs only two points in the first slope to determine its gain and offset, then one point each in the following slopes to determine their gain.

In Fig. 3 the noise margin between the photon shot noise on the CCD and the quantization noise due to the bit size of the A/D converter is shown. The plot also demonstrates the advantage of a multi-slope integrator followed by a 12-bit A/D over a standard linear 16-bit converter for small signals. Since the dynamic range of modern CCDs is often greater than 16 bits, a linear converter is forced to a larger number of bits or to undersample the read noise..

2.4 The pipeline A/D converter

To sample the output of the multi-slope integrator a 13-bit A/D converter has been implemented. We chose a 13-bit range with a fixed negative offset of 4k electrons to eliminate the need to remove the CCD offset voltage. The range of the 13-bit A/D converter is adequate to fully sample the CCD output signal, and any offset subtraction can be done later in the digital domain.

After studying several A/D architectures, we decided on a pipeline architecture for the CRIC II chip. This architecture achieves high resolution while maintaining low power consumption. It also has the advantage of 12 identical stages, greatly reducing layout efforts. Pipeline A/D converters have excellent linearity by design, as can be seen in the test results section. To prevent the digital noise from degrading the signal the A/D converter is clocked at pixel read rate and the timing is designed so that no transitions occur during either integration period. Since any digital noise is generated while the integrator is off, such noise is completely rejected.

2.5 The voltage reference

The primary function of the voltage reference is to generate a low-noise ultra-stable reference for the input stage. The same voltage is used in the A/D converter, but requirements are less strict there. The voltage reference has been optimized to give very similar performance at room temperature and at the planned operating temperature of -130 C, not to give the minimal temperature coefficient at the designed operating temperature. The plot in Fig. 4 shows excellent stability, ~0.1 mV/K at both room and operating temperature.

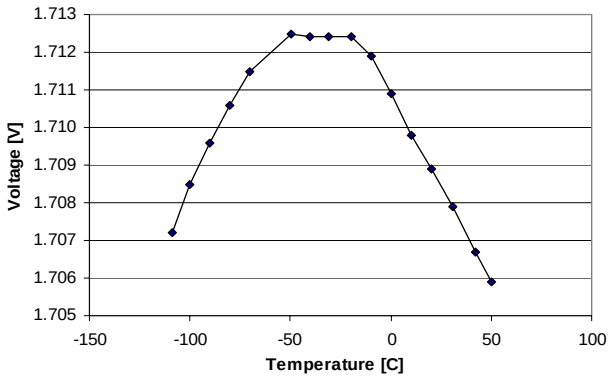

Figure 4. Voltage reference performance over temperature.

Since band-gap based voltage references are notoriously noisy, a trick had to be used to achieve the required noise performance. A sample and hold circuit was implemented at the output of the voltage reference. At the beginning of each pixel read the reference voltage is ‘frozen’ on the sample capacitor and the voltage reference is disconnected for the entire duration of

the pixel read. Therefore the entire voltage reference noise is rejected by the CDS. Only the buffer amplifiers distributing the reference voltage over the chip contribute to the reference voltage noise.

3. MEASUREMENT RESULTS

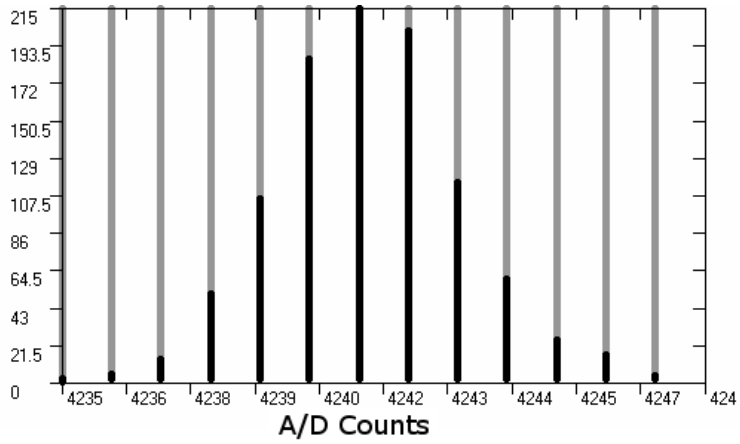

Figure 5. Noise histogram from 10000 samples at -110 C.

Proving the low noise capabilities of the CRIC II chip was one of the main testing goals. Fig. 5 shows 1.9 ADU rms noise that was measured running the chip at cold temperatures at 100k samples per second. This translates to about 6.5μV rms noise, or slightly less than two electrons. The warm performance is slightly worse due to higher thermal noise. At room temperature, we measured 2.3 ADU or 8.3μV rms noise. All noise measurements were done using the highest integrator gain. For larger signals at lower integrator gains, the noise is no longer dominated by the input stage, but by the A/D converter. For signals greater than 4k electrons, we measured 0.8 ADU or 12.8 electrons rms noise. For signals above 64k electrons we measured 0.9 ADU or 28.8 electrons rms noise, both very close to the quantization noise plotted in Fig. 3.

The linearity of a pipeline A/D converter is very good by design. Fig. 6 shows well below 1 ADU rms nonlinearity for a signal that varies over the full scale of the middle slope of the multi-slope integrator.

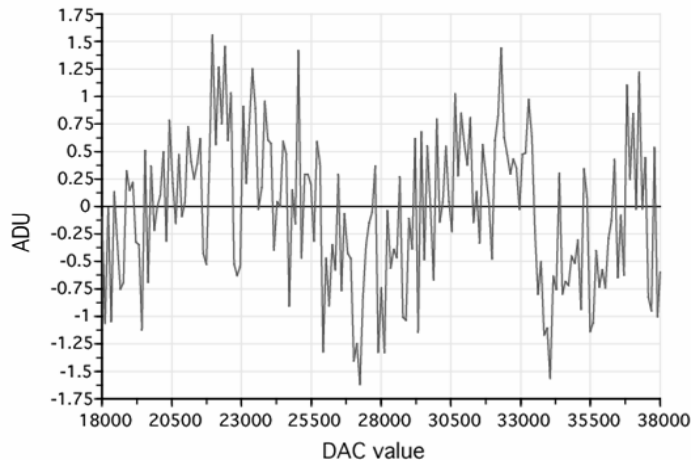

Figure 6. The integral nonlinearity is shown as the deviation from a line fit as a function of the injected charge.

The power consumption of the system is 17 mW/channel at 100 kHz. The power draw is roughly equally distributed among the analog input stage and the pipeline A/D. Our CCDs typically dissipate just as much power in the source follower load.

4. OUTLOOK

We are very pleased with the performance of the CRIC II chip. The third generation chip is in design. This will incorporate internal time sequencing and a 14-bit A/D with auto calibration. This will greatly simplify the interface and pinout of the chip. We also continue to develop a second ASIC that contains DC bias voltage DACs, timing generation and clock line drivers.

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